Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A code-divisional access (CDMA) receiver for de-scrambling and de-spreading a received signal ~~having in-phase and quadrature components~~ that was scrambled by a complex scrambling code into a first integrator input and a second integrator input, the received signal having in-phase and quadrature components, wherein the first integrator input and the second integrator input estimate a first and second communication signal that were scrambled by first and second scrambling codes, respectively, the CDMA receiver comprising:

a summer for producing a sum signal by adding the in-phase and quadrature components of the [[transmitted]] received signal;

a substractor for producing a difference signal by computing the difference between the in-phase component and the quadrature component;

a selector for selecting one of the sum and difference signals to be an imaginary component based on the complex scrambling code and for selecting one of the sum and difference signals not selected to be the imaginary component to be a real component;

a first selectable negation circuit for producing a first integrator input by selectively negating the real and imaginary components based on the complex [[spreading]] scrambling code and the first [[spreading]] scrambling code; and

a second selectable negation circuit for producing a second integrator input by selectively negating the real and imaginary components based on the complex [[spreading]] scrambling code and the second [[spreading]] scrambling code.

2. (Currently amended) The CDMA receiver of claim 1, wherein the difference signal is equal to the in-phase component minus the quadrature component.

3. (Currently amended) The CDMA receiver of claim 2, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the sum signal is selected as the imaginary component ~~is selected as the sum signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of a different value, and the difference signal is selected as the imaginary component ~~is selected as the difference signal~~ if a bit of the scrambling real

component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of the same value.

4. (Currently amended) The CDMA receiver of claim 3, wherein if the difference signal is selected as the imaginary component ~~is selected as the difference signal~~, the imaginary component is negated.

5. (Currently amended) The CDMA receiver of claim 1, wherein the difference signal is equal to the quadrature component minus the ~~quadrature~~ in-phase component.

6. (Currently amended) The CDMA receiver of claim 5, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the sum signal is selected as the imaginary component ~~is selected as the sum signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of a different value, and the difference signal is selected as the imaginary component ~~is selected as the difference signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of the same value.

7. (Currently amended) The CMDA receiver of claim 6, wherein if the sum signal is selected as the imaginary component ~~is selected as the sum signal~~, the imaginary component is negated

8. (Currently amended) The CDMA receiver of claim 1, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component and wherein the real and imaginary components are negated to produce the first integrator input if a bit of the scrambling real component of the complex scrambling code and a corresponding bit of the first [[spreading]] scrambling code are of a different value.

9. (Currently amended) The CDMA receiver of claim 1, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the real and imaginary components are negated to produce the second integrator input if a bit of the scrambling real component of the complex scrambling code and a corresponding bit of the second [[spreading]] scrambling code are of a different value.

10. (Currently amended) A method of de-spreading a received signal ~~having in-phase and quadrature components~~ that was scrambled by a complex scrambling code into de-scrambled first and second communication signals, the received signal having in-phase and quadrature components, wherein the first and second communication signals were spread by first and second spreading codes, respectively, the method comprising:

producing a sum signal by adding the in-phase and quadrature components of the [[transmitted]] received signal;

producing a difference signal by computing the difference between the in-phase component and the quadrature component;

selecting one of the sum and difference signals to be an imaginary component based on the complex scrambling code;

selecting the one of the sum and difference signals not selected to be the imaginary component to be a real component;

producing a first integrator input by selectively negating the real and imaginary components based on the complex [[spreading]] scrambling code and the first [[spreading]] scrambling code; and

producing a second integrator input by selectively negating the real and imaginary components based on the complex [[spreading]] scrambling code and the second [[spreading]] scrambling code.

11. (Currently amended) The method of claim 10, wherein the difference signal is equal to the in-phase component minus the quadrature component.

12. (Currently amended) The method of claim 11, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the sum signal is selected as the imaginary component ~~is selected as the sum signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of a different value, and the difference signal is selected as the imaginary component ~~is selected as the difference signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of the same value.

13. (Currently amended) The method of claim 12, wherein if the difference signal is selected as the imaginary component ~~is selected as the difference signal~~, the imaginary component is negated.

14. (Currently amended) The method of claim 10, wherein the difference signal is equal to the quadrature component minus the ~~quadrature~~ in-phase component.

15. (Currently amended) The method of claim 14, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the sum signal is selected as the imaginary component ~~is selected as the cum signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of a different value, and the difference signal is selected as the imaginary component ~~is selected as the difference signal~~ if a bit of the scrambling real component and a corresponding bit of the scrambling imaginary component of the complex scrambling code are of the same value.

16. (Currently amended) The method of claim 15, wherein if the sum signal is selected as the imaginary component ~~is selected as the sum signal~~, the imaginary component is negated.

17. (Currently amended) The method of claim 10, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the real and imaginary components are negated to produce the first integrator input if a bit of the scrambling real component of the complex scrambling code and a corresponding bit of the first [[spreading]] scrambling code are of a different value.

18. (Currently amended) The method of claim 10, wherein the complex scrambling code has a scrambling real component and a scrambling imaginary component, and wherein the real and imaginary components are negated to produce the second integrator input if a bit of the scrambling real component of the complex scrambling code and a corresponding bit of the second [[spreading]] scrambling code are a different value.